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DESIGN AND SYNTHESIS OF TERNARY LOGIC ELEMENTS

The aim of this paper is creating some ternary elements. The threshold element of ternary logic on bipolar transistors and elements of ternary systems based on it are considered. The main disadvantages of this approach are identified. The multi-threshold element of multivalued logic and its specific four-threshold implementation are considered. The scientific nowelty is the using of a multithreshold element of multivalued logic as a basis for constructing elements of ternary systems. It is shown that the advantages of a multi-threshold element of multi-valued logic are a larger number of thresholds of input signals, a larger number of levels that it can distinguish and a larger number of output signals. The implementation of some ternary elements, such as half-adder, disjunction and strong conjunction, is given. The practical significance of obtained results is that the multithreshold element of multivalued logic allows us to use it for synthesis basic elements of ternary logic and use one approach for all of them. Additional practical advantage is that in practice it allows you to build more diverse logical and arithmetic devices with a simplified implementation. The implementation of ternary devices based on threshold logic is a way to create ternary devices that can compete with binary devices in terms of equipment, capacity, operational capabilities, and variety. This, in turn, leads to greater speed and simplification of the structure of devices, as well as increasing the speed of data processing. These advantages are significant in such areas of computer use as intelligent data processing systems, expert systems, decision theory, i.e., where data analysis is performed. Prospects for further research are to use the method of construction and synthesis of nodes of ternary computer systems, based on MTEML. Their optimization, and development of principles of mathematical modeling and software of such systems and their elements is expedient.

Keywords: ternary logic, threshold element of ternary logic, multi-threshold element of multi-valued logic, disjunction, strong conjunction

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ПРОЕКТУВАННЯ ТА СИНТЕЗ ТРІЙКОВИХ ЛОГІЧНИХ ЕЛЕМЕНТІВ

Метою роботи є створення деяких трійкових елементів. В роботі розглянуто пороговий елемент трійкової логіки на біполярних транзисторах та елементи трійкових систем на його основі. Визначено основні недоліки такого підходу. Розглянуто багатопороговий елемент багатозначної логіки та його конкретну чотирипорогову реалізацію. Наукова новизна полягає у використанні багатопорогового елемента багатозначної логіки як основи для побудови елементів трійкових систем. Показано, що перевагами багатопорогового елемента багатозначної логіки є більша кількість порогів вхідних сигналів, більша кількість рівнів, які він може розрізнити, і більша кількість вихідних сигналів. Наведено реалізацію деяких трійкових елементів, таких як напівсуматор, диз'юнкція та сильна кон'юнкція. Практичне значення отриманих результатів полягає в тому, що багатопороговий елемент багатозначної логіки дозволяє використовувати його для синтезу базових елементів трійкової логіки та використовувати один підхід для всіх них. Додаткова практична перевага полягає в тому, що на практиці це дозволяє будувати більш різноманітні логічні та арифметичні пристрої зі спрощеною реалізацією.

Реалізація трійкових пристроїв на основі порогової логіки – це спосіб створення трійкових пристроїв, які можуть конкурувати з двійковими пристроями за кількістю обладнання, потужністю, експлуатаційними можливостями та різноманітністю. Це, в свою чергу, призводить до більшої швидкості та спрощення структури пристроїв, а також збільшення швидкості обробки даних. Ці переваги є значущими в таких сферах використання комп'ютерів, як інтелектуальні системи обробки даних, експертні системи, теорія прийняття рішень, тобто де проводиться аналіз даних. Перспективами подальших досліджень є використання методу побудови та синтезу вузлів потрійних комп'ютерних систем на основі MTEML. Доцільною є їх оптимізація, розробка принципів математичного моделювання та програмного забезпечення таких систем та їх елементів.

Ключові слова: трійкова логіка, пороговий елемент трійкової логіки, багатопороговий елемент багатозначної логіки, диз'юнкція, сильна кон'юнкція.

Introduction

Ternary logic for computers, introduces its units of information: trit and trite (like binary bit and byte). Trit (approximately 1,585 bits) is a ternary digit in the ternary number system. Trite is the minimum ternary word addressed in the memory of a ternary computer. Often, one trite is equal to six trits.

In digital electronics, the "bit" is implemented by the minimum logical element of a binary computer - a binary trigger. Trit is implemented by a ternary trigger, which can simultaneously operate with three values at once, instead of two as in the binary trigger. One trite can encode 729 values at 6 trits, against 256 one byte at 8 bits. It takes values from the range of -364 to 364, in contrast to the byte range 0 - 255. This allows you to process much more information in one CPU clock [1].

The practical feasibility of ternary technology is not yet clear. The ternary technique is equivalent to the binary technique in the sense that everything feasible in one of them, with one or another approximation can be done in another. It is also clear that ternary elements must be more complex and expensive than binary, and ternary logic is clearly more complex than binary. But, on the other hand, and more diverse, ternary memory is more powerful, and the operational capabilities of ternary valves are richer.

Data processing in the conditions of ternary technology should be carried out at the same physical speed of the elements faster, and the structure of the ternary device, as a rule, is simpler than the structure of a functionally equivalent binary device. In other words, the ternary technique is characterized in comparison with the binary complication of the elements, which makes it possible to simplify the structures created from them, reduce the number of communication lines, and increase the speed of data processing.

Thus, it is obvious that ternary technology and systems based on it are more efficient and convenient than binary in intelligent systems, in expert systems, in decision making theory.

Related works

To date, the element base of ternary systems, as well as the ternary systems themselves, is at the stage of its development. Various solutions and methods for constructing ternary elements are proposed [2]. There are different approaches and principles of their construction [3]. Consider some of them.

Threshold element on bipolar transistors

The implementation of a ternary logic element on bipolar complementary unsaturated transistors - a threshold element of ternary logic (TETL) is known [4]. The element is implemented based on a binary ECL-element, the circuit of which is supplemented by its replica on complementary transistors. TETL consists of a block of emitter repeaters (BER) and connected to its outputs m blocks of current switches (CS.1… CS.m). BER is implemented on two repeaters, respectively on n-p-n and p-n-p transistors. The first repeater is connected between the common bus and the power bus "-E", the second - between the power bus "+ E" and the common bus. Each CS unit contains 2 current switches. Fixed currents If are formed by two current sources connected in accordance with the power buses "+ E" and "-E".

The disadvantage of TETL is that a small number of thresholds is determined, because of which the levels "++" = "0+" and "- -" = "0-" do not differ.

However, the circuit and structural solutions used in them and tested in practice can find application in modern digital technology.

Devices based on TETL

Some devices of ternary logic are realized on the basis of TETL, such as the former of three-digit constants, ternary repeater, non-cyclic inverter, the scheme "OR".

The device for forming constants (FC) has 2 outputs: +1 and -1 [5,7]. At any input ternary value, the outputs are constantly exposed to +1 and -1 (discrete currents of a fixed value + If and -If). The purpose of FC is to set a constant triple value at the right points of the scheme: +1 and -1. In this way, the desired point of the device is tied to a given logical value.

The two-input circuit "OR" has two outputs - direct and inverse.

Let`s consider in detail a ternary half-adder, which was implemented on the threshold elements. The corresponding truth table is presented in table 1.

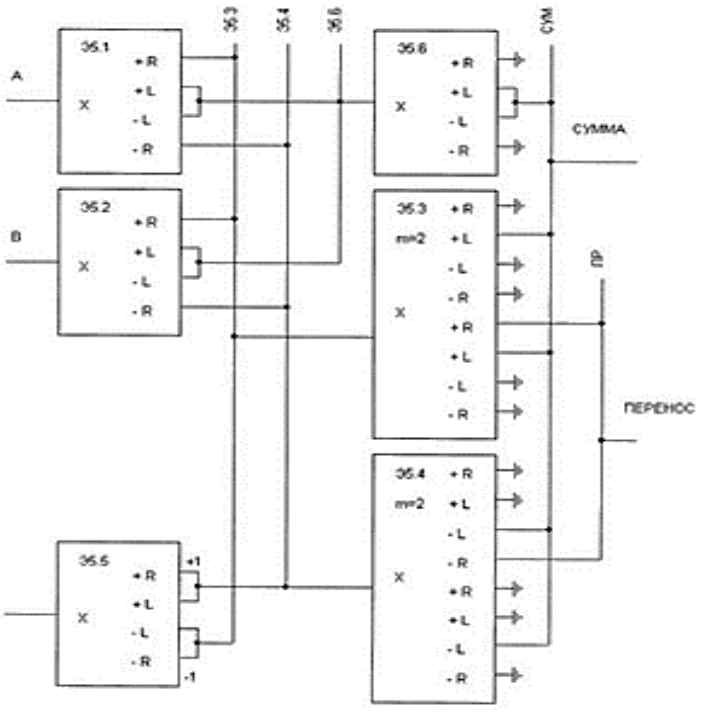

Fig. 1: Triple half-adder on the basis of TETL

This circuit contains five identical elements with one block of current switches (m = 1): E5.1, E5.2, E5.3, E5.4, E5.5 and two identical elements with two blocks of current switches (m = 2): E5.3, E5.4 as it`s shown on Fig. 1. Elements E5.1 and E5.2 divide the ternary variables A and B into their two-digit components. Element E5.5 is used as a constant shaper.

For the final formation of the SUM signal, a double inverted TRANSFER signal is fed to the SUM bus, which is formed by combining the signals of the same name + L and –L from the outputs of elements E5.3 and E5.4. For doubling (formation of signals + 2If and -2If) in elements E5.3 and E5.4 use two current switches and two sets of outputs (m = 2).

Table 1

Truth table for ternary half-adder

№	a	b	S	C
1	-	-	+	-
2	-	0	-	0
3	-	+	0	0
4	0	-	-	0
5	0	0	0	0
6	0	+	+	0
7	+	-	+	0
8	+	0	0	0
9	+	+	-	+

a, b - input signals, S - the sum of the input signals, C - overflow, positive for two positive input signals, and negative - for two negative input signals.

Also, a node of ternary circuitry (Fig. 2), consisting of 3 PETL was built on the basis of TETL [5].

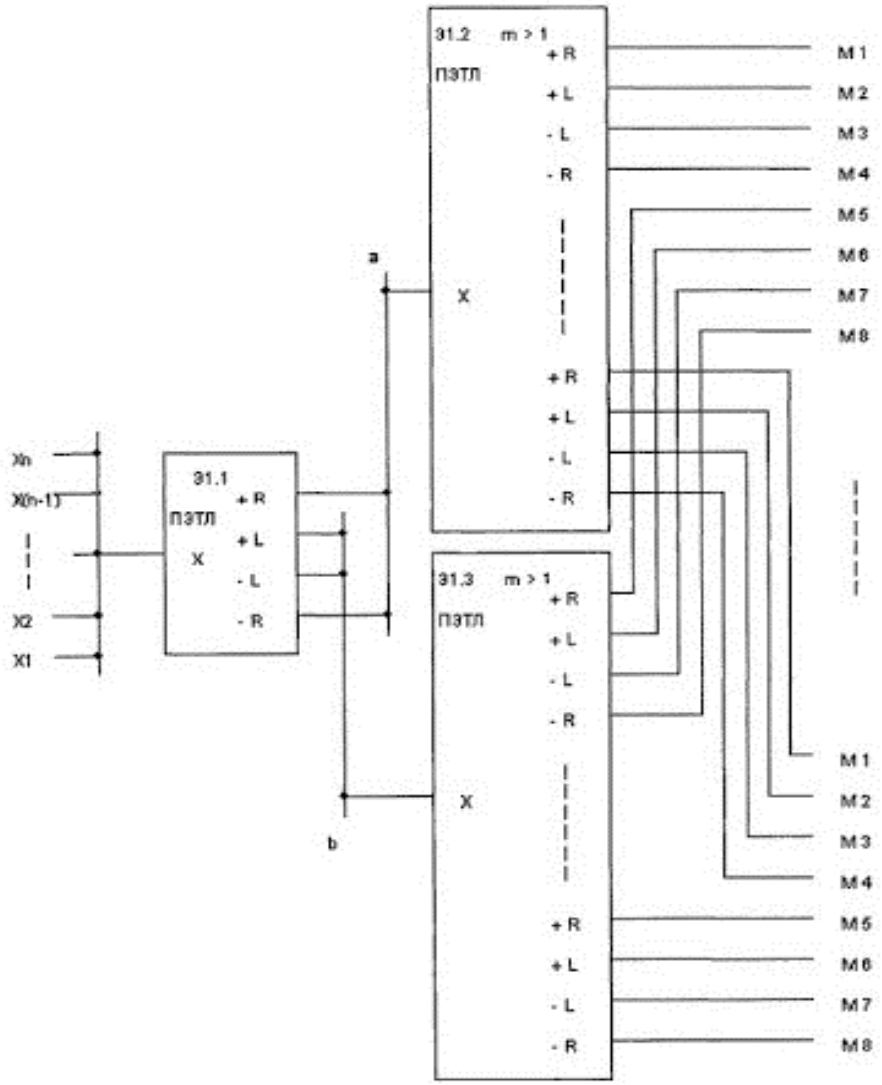

Fig. 2: Node of ternary circuitry

Another device built on the basis of TETL is a triple reversing shift register.

The nodes of this element consist of a TETL and for them everything related to the TETL is valid: the inputs algebraically sum up the triple values; nodes can have more than one group of outputs [6].

Triple Reverse Offset Register operates with data presented in a ternary code with numbers +1, 0 and -1, and implements the following functions:

- storage of k-bit ternary values;
- parallel writing and reading;
- consecutive writing and reading;
- shift right and left by a specified number of digits.

Considering the devices built on the basis of TETL, we can conclude that all these elements do not allow the full implementation of ternary logic, do not have a common approach to its implementation, and complicate the implementation of ternary devices and their structure. Therefore, the issue of developing a standard approach and methods for the synthesis of ternary elements is quite relevant.

Proposed technique

Multithreshold element of multivalued logic

To solve this problem, let's consider a multi-threshold element of multivalued logic [8] as a basic element for constructing elements of multivalued systems, including ternary. Its block diagram is shown in Fig. 3.

Consider in detail its structure and principle of operation. Block 1 is a block of threshold formation (BTF), 2.1… 2.n - emitter repeaters, 3.1 … 3.m - current switches. The input of the threshold formation unit receives k discrete current signals Ij from the previous elements. They can take one of the typical values (for example, for the binary logic of such values will be two: Ij = +1, Ij = 0; for a ternary symmetric system of such values will be three: Ij = +1, Ij = 0, Ij = –1).

$$k = k_{+1} + k_{-1} + k_0,$$

where k_{+1} – the number of signals whose current values +1,
k_{-1} – the number of signals whose current values -1,
k_0 – the number of signals whose current values 0.

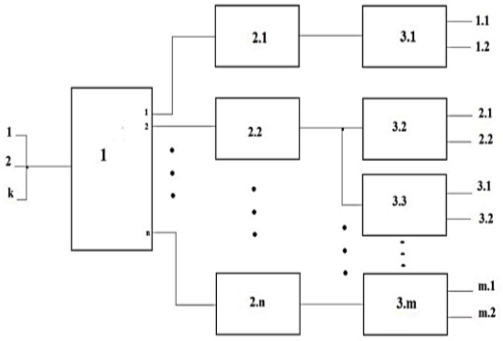

Fig. 3: Block diagram of MTEML

BTF forms n thresholds in one turn. Its outputs are fed to the inputs of emitter repeaters (ER) 2.1… 2.n. Active ER generate signals on the connected current switches (CS) 3.1… 3.m.

Features of the structure of MTEML: the element does not operate with potential, but with current values of signals, so the outputs of MTEML can be combined in any number, but the signal can be applied only to the input of one element; ability to form any number of thresholds that MTEML can distinguish.

The number of BTF thresholds depends on the number of levels of the input variable that the MTEML is able to distinguish and, accordingly, the bit size of the variable or the complexity of the operations that can be performed. In order to form the logic of the operation of this element, you need to combine the outputs of the CS in the required combination.

Four-threshold implementation of MTEML

Consider an example of the implementation of MTEML for a ternary symmetric system - its four-threshold version [9], the block diagram of which is shown in Fig. 4.

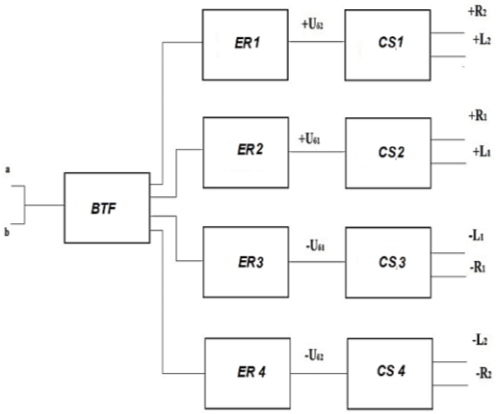

Fig. 4: Block diagram of the four-threshold MTEML

The values of voltages generated at the outputs of the ER and respectively fed to the inputs of current switches are given in table. 2. In this table "1" is an active signal (affects the CS), "0" is an inactive signal (does not affect the CS) at the output of the corresponding ER.

Table 2

Voltages generated at the output of emitter repeater blocks

The sum of the input currents (terlev)	ER1 (+ $U_{б2}$)	ER2 (- $U_{б2}$)	ER3 (+ $U_{б1}$)	ER4 (- $U_{б1}$)
– –	1	0	1	0
–	0	0	1	0
0	0	0	0	0
+	0	0	0	1
++	0	1	0	1

If the signal at the input of the CS is active, the output L of the corresponding CS current is generated, otherwise - the current is generated at the output R. CS together have 8 outputs, a combination of which can form the necessary logical or arithmetic functions [10].

The values of the output signals of the CS depending on the input currents are described by the terlev function, given in table 3.

Table 3

The values of the outputs (output currents) of the current switches CS1 – CS4

The sum of the input currents	Output signals of current switches							
	CS 1		CS2		CS3		CS4	
terlev	+R2	+L2	–R2	–L2	+R1	+L1	–R1	–L1
– –	0	+	–	0	0	+	–	0
–	+	0	–	0	0	+	–	0
0	+	0	–	0	+	0	–	0
+	+	0	–	0	+	0	0	–
+ +	+	0	0	–	+	0	0	–

The implementation of MTEML for ternary symmetric logic, in comparison with TETL, has several advantages: 4 thresholds of input signals (in TETL - 2), distinguishes 5 levels (in TETL - 3), has 8 output signals (in TETL - 4). All this together allows you to build more diverse logical and arithmetic devices with a simplified implementation.

Experiments

Elements of ternary systems based on a multi-threshold element of multivalued logic

Triple half-adder

Based on MTEML the ternary half-adder was constructed [11] which structural scheme is shown in fig. 5.

The input of the BFT 1 receives two ternary variables a and b. BFT forms four symmetrical thresholds. The outputs of the BFT are fed to the emitter repeaters ER1 - ER4, at the output of which voltages are formed, depending on the input function terlev, which are given in table 2.

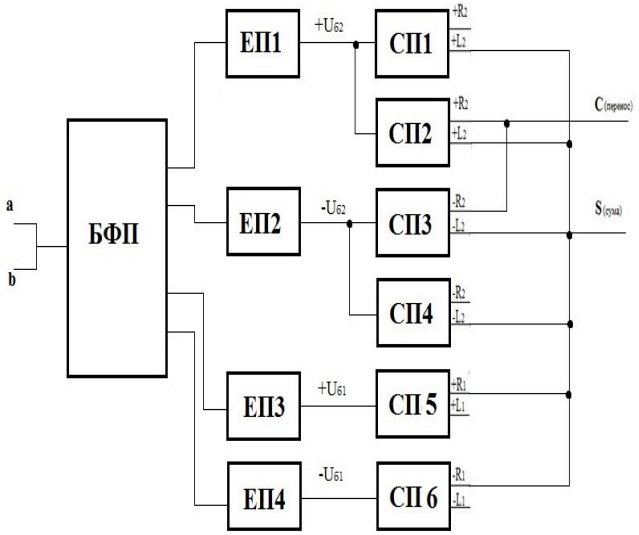

Fig. 5: Block diagram of a ternary half-adder based on MTEML

The table 4 shows the values of the outputs of the CS depending on the function terlev. This function illustrates the transformations performed by a multi-threshold element of multivalued logic, based on which a ternary half-adder is constructed [12].

Using table 4, it is possible to construct operations of addition on the module 3 - S and transfer - C (table 5).

Table 4

The values of the outputs (output currents) of the current switches CS1 - CS6

The sum of the input currents	Output signals of current switches							
	CS 1, CS2		CS3, CS4		CS5		CS6	
terlev	$+R_2$	$+L_2$	$-R_2$	$-L_2$	$+R_1$	$+L_1$	$-R_1$	$-L_1$
– –	0	+	–	0	0	+	–	0
–	+	0	–	0	0	+	–	0
0	+	0	–	0	+	0	–	0
+	+	0	–	0	+	0	0	–
+ +	+	0	0	–	+	0	0	–

From the table 4 it follows that :

$$S = 2(+L_2(ab), -L_2(ab)) + (+R_1(ab), -R_1(ab))$$
$$C = (+R_2(ab), -R_2(ab))$$

The constructed ternary half-adder contains fewer elements and has a simplified circuit design solution, due to the fact that it is built on the basis of MTEML.

Table 5

Truth table of ternary half-adder

a	b	terlev	S	$2(+L_2(ab), -L_2(ab))$	$+R_1(ab), -R_1(ab)$	C	$+R_2(ab), -R_2(ab)$
–	–	– –	+	++	–	–	–
–	0	–	–	0	–	0	0
–	+	0	0	0	0	0	0
0	–	–	–	0	–	0	0
0	0	0	0	0	0	0	0
0	+	+	+	0	+	0	0
+	–	0	0	0	0	0	0
+	0	+	+	0	+	0	0
+	+	++	–	– –	+	+	+

In order to demonstrate this, it is necessary to bring the TETL-based half-adder to a form similar to the constructed ternary half-adder (Fig. 6).

The naked eye can see from the diagram that the structure of the half-adder based on the TETL is much more complex. The number of elements in it is much larger. As well as many unused outputs.

The structure of the ternary half-adder on the basis of TETL consists of six threshold elements of ternary logic, which in turn contain a block of threshold formation, emitter repeaters and current switches. In total we receive 38 elements.

The proposed ternary half-adder is built on the basis of only one multi-threshold element of multi-valued logic, which allows the use of only 11 elements. That is, the proposed scheme contains more than 3 times less logical elements.

Disjunction and strong conjunction

On the basis of MTEML the structures of elements of realization of some ternary functions, namely - disjunctions and strong conjunctions were constructed.

A two-threshold MTEML is sufficient to construct a disjunction, while a four-threshold MTEML is required to construct strong conjunctions.

The values of the outputs (truth tables) of these functions are given in table 6 and table 7, and block diagrams in Fig. 7 and fig. 8 respectively.

The tables show which current switchers outputs need to be combined in block diagrams to obtain disjunction and strong conjunction functions.

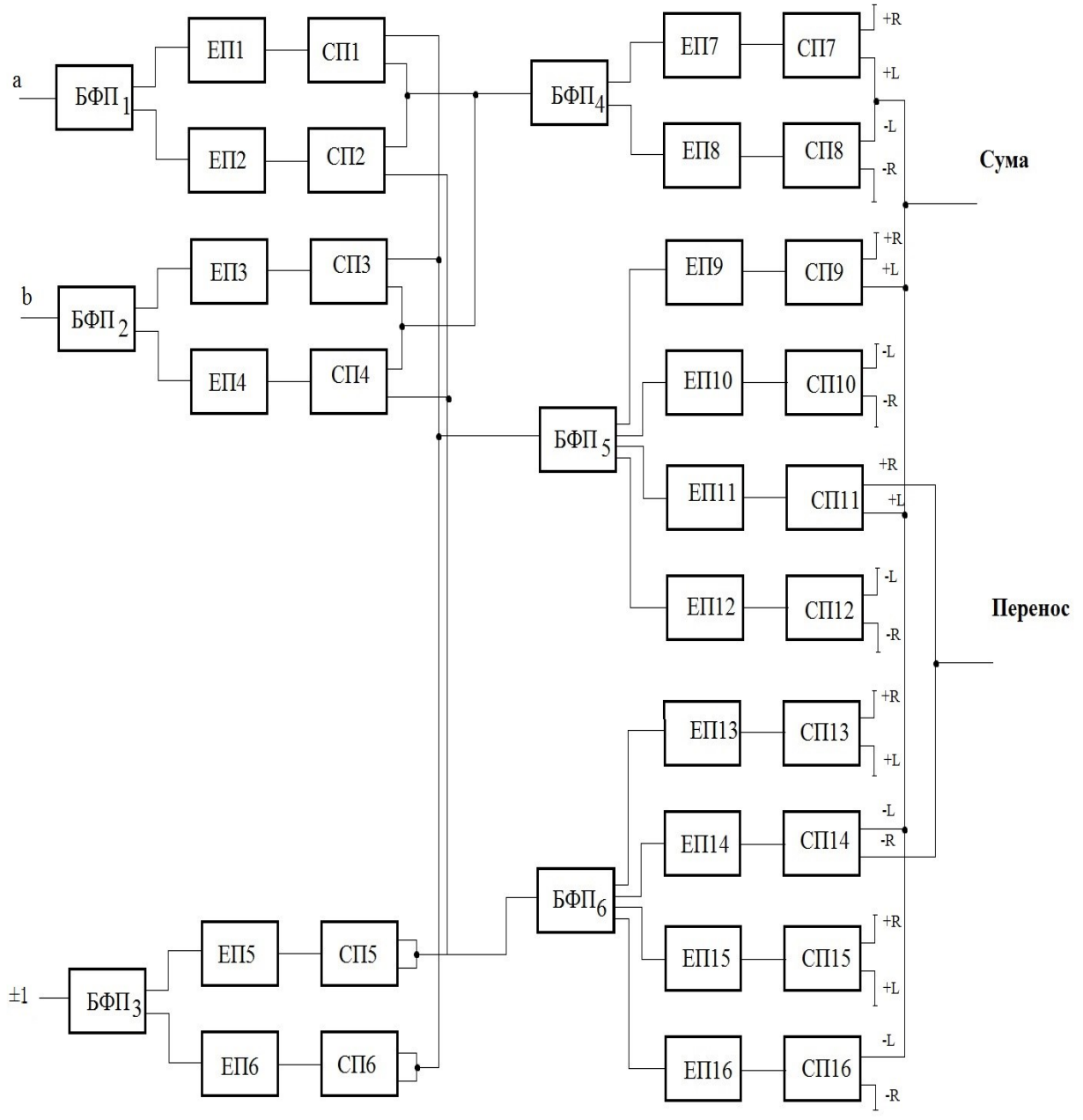

Fig. 6: The structure of the ternary half-adder on the basis of TETL, reduced to a form similar to the half-adder built on the basis of MTEML

Table 6

Table for constructing a ternary disjunction

a	b	terlev	$a \vee b$	$+\mathbf{R_1}(ab)$	$-\mathbf{R_1}(ab)$
–	–	– –	–	0	–
–	0	–	–	0	–
–	+	0	0	+	–
0	–	–	–	0	–
0	0	0	0	+	–
0	+	+	+	+	0
+	–	0	0	+	–
+	0	+	+	+	0
+	+	++	+	+	0

Table 6 shows us, that to obtain the disjunction a∨b it is necessary to combine the outputs $+R_1$ та $-R_1$, , ie we can write:

$$a \vee b = +R_1(ab);\ -R_1(ab), \text{or reduced: } a \vee b\ =\ +R_1;\ -R_1$$

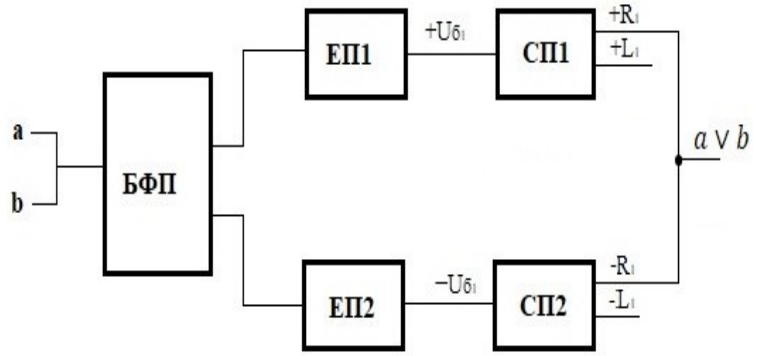

Fig. 7: Ternary disjunction

Table 7

Strong conjunction table

a	b	terlev	$a\&_L b$	$-\mathbf{R_2}(ab)$	$+\mathbf{R_1}(ab)$	$-\mathbf{R_1}(ab)$	$+\mathbf{L_1}(ab)$
–	–	– –	–	–	0	–	+
–	0	–	–	–	0	–	+
–	+	0	–	–	+	–	0
0	–	–	–	–	0	–	+
0	0	0	–	–	+	–	0
0	+	+	0	–	+	0	0
+	–	0	–	–	+	–	0
+	0	+	0	–	+	0	0
+	+	++	+	0	+	0	0

To obtain a strong conjunction a&b it is necessary to combine the outputs $-R_2$, $+R_1$, $-R_1$, $+L_1$, i.e. we can write

$$a\&b = -R_2;\ +R_1;\ -R_1;\ \ +L_1$$

In this case, we see that the signal -R2 is used to obtain a strong conjunction, which is fundamentally absent in the TETL.

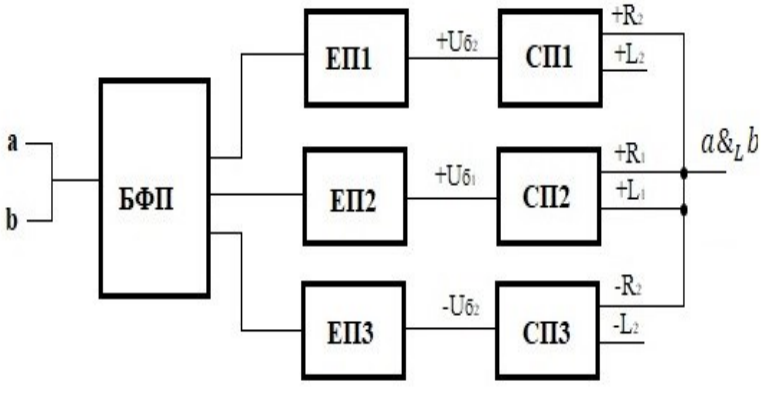

Fig. 8: Block diagram of a strong conjunction

Conclusions

Thus, the threshold element of ternary logic on bipolar unsaturated transistors and such elements of ternary systems based on it as the shaper of three-digit constants, ternary repeater, non-cyclic inverter, "OR" circuit are considered. All these elements do not allow to fully implement ternary logic, do not have a general approach to its implementation, and have a complex structure, which complicates the implementation of ternary devices. The multi-threshold element of multivalued logic and its specific four-threshold implementation allows to obtain ternary elements of relatively simple structure with a more generalized approach to their implementation. The use of a multithreshold element of multivalued logic as a basis for the construction of elements of ternary systems is proposed, the advantages of its use are determined. The realization of half-adder, disjunction and strong conjunction is given.

The implementation of ternary devices based on threshold logic is a way to create ternary devices that can compete with binary devices in terms of equipment, capacity, operational capabilities, and variety. This, in turn, leads to greater speed and simplification of the structure of devices, as well as increasing the speed of data processing. These advantages are significant in such areas of computer use as intelligent data processing systems, expert systems, decision theory, i.e., where data analysis is performed.

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